REMARKS

This amendment responds to an Office Action dated March 20, 2002. Claims 1-20 are pending in the application. Claims 1-20 were rejected under 35 U.S.C §112, first paragraph. No claims were allowed.

The Examiner stated that "the 'consisting essentially of' language is not supported in that it excludes additional steps that were not excluded in the original specification." The examiner based this rejection on the last paragraph of the original specification. The Applicant has amended the claims to remove the "consisting essentially of" language, so that the §112 rejection is now moot. However, Applicant does not concede the argument made by the examiner that a general concluding paragraph that references the possibility of additional steps or elements, indicates that the Applicant was not in possession of an embodiment that excludes those additional elements. Especially where some of the described embodiments do not contain additional elements.

The remainder of the remarks are directed to rejections made in the previous Office Action dated July 13, 2001, as it was those rejections that initially prompted the inclusion of the "consisting essentially of" language.

The Office Action dated July 13, 2001 rejected claims 1-20 as being unpatentable over Kodera *et al.* (US 5,445,996) in view of Grover *et al.* (US 5,759,917) and further in view of Burke *et al.* (US 5,934,978). No claims have been allowed.

Applicant has amended the claims to further clarify the scope of the invention. Applicant's invention provides a method of fabricating

integrated circuit structures using CMP that provides an ability to polish a silicon dioxide layer such that the high structure areas are polished as substantially the blanket polishing rate and low structure areas are polished at an essentially zero polishing rate, without the use of dummy structures deposited onto the silicon dioxide to control the polishing characteristics. Support for the exclusion of dummy structures can be found in the original specification as filed on page 7, lines 6-9. It should be noted that the background, on page 1, lines 14-18, the use of dummy structures for controlling the CMP rate is presented as a prior art solution, which places unacceptable restrictions on the design and functionality of IC devices. The modification of the ceria slurry as provided in the present invention addresses the ability to achieve the desired polishing capability without the need for dummy structures.

To establish a prima facie case of obviousness, three basic criteria must be met. There must be some teaching or suggestion to modify the reference or combine reference teachings. There must be a reasonable expectation of success. The prior art references must teach or suggest all claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicants' disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Applicant is aware that one cannot show nonobviousness by attacking references individually where the rejections are based on a combination of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). However, just as the Examiner discussed each reference in turn and then discussed the combination of these references in support of an

obviousness rejection, Applicant will likewise discuss the short comings of each reference as well as the lack of suggestion, or motivation, to combine the references to achieve a process having all of the claim limitations.

It has been asserted, by referring to Figs. 22-27 that Kodera discloses polishing recessed areas at near a zero polishing rate until the raised portions were reduced to almost that of the recessed portion. Then both portions were polished together.

However, the polishing shown in Figs. 22-27 are based upon polishing the structure as shown in Figs 21A-21E. Fig. 21D clearly shows a polysilicon film 208 overlying the silicon dioxide. The polysilicon film 208 is also referred to as a stopper film. It is clear from the description in Kodera that it is being used as a dummy structure, similar to that described in Applicant's background, to affect the polishing behavior. See Column 24, line 66 through Column 25, line 23; and Column 26, lines 52-58, which state:

> "As described heretofore in detail, the above mode of carrying out the method of the present invention is not accompanied by the problem of dishing nor any additional process steps to planarize a film **because the film to be polished is planarized by polishing the film to be planarized simultaneously with a stopper film that has been formed on the film to be planarized**." (emphasis added).

Kodera et al. teaches the polishing of a polysilicon film, which is more resistive to polishing than silicon dioxide, and a silicon dioxide film together to reduce the polishing rate of low areas in order to avoid dishing. Col. 24, lines 32-41. Once the polysilicon film is polished off of the higher structures, the underlying SiO_2 film is polished at a faster rate than the polysilicon film remaining over the low areas. In other

words Kodera *et al.* uses a polysilicon dummy structure, which is referred to in Kodera as a stopper. The benefits of a dummy structure are further summarized in Col. 26 lines 52-58, which specifies that the film to be planarized and the stopper layer (a.k.a. dummy structure) are planarized simultaneous, and Col. 27 lines 22-38. Kodera *et al.* teaches modification of the device structure by applying a dummy structure as the means of achieving desired polishing behavior. Kodera *et al.* fails to teach or suggest, even in combination with Grover *et al.* or Burke *et al.*, modifying the slurry in any way to achieve the desired polishing behavior. Kodera *et al.* uses a dummy structure whereas Applicant achieves the result by modifying the slurry. Applicant has amended the claims to more further clarify the absences of any dummy structure, such as the polysilicon overlying the silicon dioxide in Kodera *et al.* Although Kodera *et al.* describes a method for controlling the polishing of high structures and low structures, it does not teach to do so by modifying the slurry, but only through the use of a dummy structure, (i.e. the overlying polysilicon layer 208, in Fig 21D).

Although Grover *et al.* relates to the use of CMP to shallow trench isolation, Grover *et al.* addressed the issues of selectivity between silicon dioxide and silicon nitride. No teaching or suggestion has been identified in Grover *et al.* to combine it with Kodera *et al.* to polish silicon dioxide in the manner claimed by Applicant. It did not address modifying the behavior of slurry used to polish just silicon dioxide. The is no teaching or suggestion to combine Grover *et al.* with Kodera *et al.* to control the polishing rates, as both of these methods are related to two material systems and not the polishing of silicon dioxide, without a dummy structure.

Burke *et al.* addressed a means to reduce scratching and associated defects. Although it disclosed the use of ethylene glycol, it did not disclose the use of ethylene glycol to modify the polishing rates of silicon dioxide, which is Applicant's invention. There has been no suggestion to combine the teaching of the use of ethylene glycol, with those of Grover *et al.* and/or Kodera *et al.* to produce a process having all of the limitation of Applicant's claims.

The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. *In re Fritch*, 972 F.2d 1260, 23 USPQ2d 1780 at 1783-84 (Fed. Cir. 1992).

With respect to independent claim 1, Applicant has amended the claim to clarify that the silicon dioxide layer is provided without any dummy structure, and that the polishing is carried out on the silicon dioxide layer without polishing any dummy structure. As there is no teaching or suggestion in the combination of Kodera *et al.*, Grover *et al.*, and Burke *et al.* to perform the process or achieve the results of Applicant's claims without the use of a dummy structure. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 1.

Regarding dependent claims 2-4, as they depend from amended claim 1, which is allowable for the reasons discussed above, Applicant likewise requests allowance of claims 2-4.

With respect to independent claim 5, Applicant has amended the claim to clarify that the silicon dioxide layer is provided without any dummy structure, and that the polishing is carried out on the silicon dioxide layer without polishing any dummy structure. As there is no teaching or suggestion in the combination of Kodera *et al.*, Grover *et al.*,

and Burke *et al.* to perform the process or achieve the results of Applicant's claims without the use of a dummy structure. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 5.

Regarding dependent claims 6-7, as they depend from amended claim 5, which is allowable for the reasons discussed above, Applicant likewise requests allowance of claims 6-7.

As independent claims 8, 10, 13, 16, and 17 have all been amended to clarify the absence of any dummy structure, and the polishing of silicon dioxide without using any dummy structure, and for the reasons discussed above in connection with independent claim 1, Applicant respectfully requests allowance of independent claims 8, 10, 13, 16, and 17.

Regarding dependent claims 9, 11, 12, 14,15, and 18-20, as they all depend from amended independent claims, which are allowable for the reasons discussed above, Applicant likewise requests allowance of dependent claims 9, 11, 12, 14,15, and 18-20.

Accordingly, Applicant respectfully requests allowance of all claims 1-20, for the reasons discussed above.

As an attachment hereto, applicant herewith submits a copy of all amended claims showing changes by underlining and strikethrough, along with a set of amended claims in clean form incorporating all amendments entered to date or submitted herein

A request for a three-month extension of time to respond, together with a deposit account authorization covering the fee therefore, accompanies this amendment.

In view of the foregoing, the Applicant requests reconsideration of the application and submits that the application is now in allowable form and should be passed to issue.

Respectfully submitted,

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Attachment to Preliminary Amendment Accompanying Request for Continued Examination Under 37 § 1.114 Dated September 20, 2002

Application Serial No. 09/270,606
Version With Markings to Show Changes Made

1. (Twice Amended). A method of fabricating an integrated circuit using CMP ~~consisting essentially of~~comprising:

providing a substrate with an overlying ;

~~depositing~~ silicon dioxide layer ~~over the substrate~~, and without any dummy structure;

forming a CMP slurry containing cerium oxide;

adding a slurry modifier to the slurry, wherein the slurry modifier combined with CMP slurry polishes low structure areas at a substantially zero rate and polishes high structure areas at a rate approximating a blanket polishing rate without the use of a dummy structure; and

polishing the silicon dioxide layer without polishing any dummy structure using the modifier-containe~~d~~ing slurry, whereby the low structure areas are polished at a substantially zero rate and the high structure areas are polished at a rate approximating the blanket polishing rate without using any dummy structure.

5. (Twice Amended). A method of fabricating an integrated circuit using CMP ~~consisting essentially of~~comprising:

providing a substrate with an overlying ;

~~de~~positing silicon dioxide layer ~~over the substrate~~, and without any dummy structure;

forming a CMP slurry containing cerium oxide at a concentration of between about 1% and 50% by weight;

adding a slurry modifier to the slurry, wherein the slurry modifier combines with the CMP slurry to enable ~~polishes~~ polishing of low structure areas at a substantially zero rate and ~~polishes~~ polishing of high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide layer without any dummy structures using the modifier-contained slurry, whereby the low structure areas are polished at a substantially zero rate and the high structure areas are polished at a rate approximating the blanket polishing rate without using a dummy structure.

8. (Twice Amended). A method of fabricating an integrated circuit using CMP ~~consisting essentially of~~comprising:

providing a substrate with an overlying ;

~~depositing~~ silicon dioxide layer ~~over the substrate~~, and without any dummy structure;

forming a CMP slurry containing cerium oxide at a concentration of between about 1% and 50% by weight;

adding ethylene glycol at a concentration of up to 50% for polishing low structure areas at a substantially zero rate and polishing high structure areas at a rate approximating a blanket polishing rate; and

polishing the silicon dioxide layer without any dummy structure using the slurry, whereby the low structure areas are polished at a substantially zero rate and the high structure areas are polished at a rate approximating the blanket polishing rate without using a dummy structure.

10. (Twice Amended). A method of fabricating an integrated circuit using CMP ~~consisting essentially of~~comprising:

providing a substrate~~;~~

~~depositing~~ ~~with an overlying~~ silicon dioxide layer, and without any dummy structure ~~over the substrate~~ such that the silicon dioxide layer forms low structure areas and high structure areas;

forming a CMP slurry containing cerium oxide;

adding a slurry modifier to the slurry to produce a modified slurry that polishes the low structure areas at a substantially zero rate and polishes the high structure areas at a rate approximating a blanket polishing rate without relying on any dummy structure; and

polishing the silicon dioxide having high structure areas and low structure areas using the modified slurry, whereby high structure areas are polished at a rate approximating a blanket polishing rate and low structure areas are polished at a substantially zero rate.

13 (Thrice Amended). A method of fabricating an integrated circuit using CMP ~~consisting essentially of~~comprising:

providing a substrate with an overlying ;

~~depositing~~ silicon dioxide layer ~~over the substrate~~, and without any dummy structure such that the silicon dioxide layer forms low structure areas and high structure areas, without any dummy structure;

forming a CMP slurry having a high structure polishing rate lower than a blanket polishing rate;

adding a slurry modifier to the slurry to produce a modified slurry that polishes high structures at a rate approximating the blanket polishing rate; and

polishing the high structure areas of silicon dioxide, whereby the high structure areas are polished at a rate approximating the blanket polishing rate without using any dummy structure.

16. (Twice Amended). A method of chemically-mechanically polishing a silicon dioxide layer having high structure areas and low structure areas overlying a semiconductor substrate ~~consisting essentially~~comprising:

forming a slurry comprising cerium oxide and ethylene glycol; and

polishing the silicon dioxide layer, without any dummy structure, ~~only~~ such that the high structure areas are polished at a rate approximating a blanket polishing rate, and the low structure areas are polished at a substantially zero rate, without using any dummy structure.

17 (Twice Amended). A method of fabricating an integrated circuit using CMP ~~consisting essentially of~~comprising:

providing a substrate with an overlying ;

~~depositing~~ silicon dioxide layer ~~over the substrate~~, and without any dummy structure such that the silicon dioxide layer forms low structure areas and high structure areas;

forming a CMP slurry having a low-density high structure polishing rate and a high-density high structure polishing rate, wherein the low-density high structure polishing rate is essentially the same as a high-density high structure polishing rate; and

polishing the high structure areas without the use of dummy structures, whereby the polishing rate is independent of pattern density.